CLAIMS

What is claimed is:

1. A method for performing at least one operation of a testing operation and a burn-in operation on an uncut wafer having two opposing surfaces using a first plate which includes a biasing mechanism, and a second rigid plate selectively engageable with the first plate, the second rigid plate having a plurality of contact elements extending therefrom and having a cavity for receiving the uncut wafer therein, the method comprising:

providing a wafer having a plurality of semiconductor die thereon and at least one interconnect between at least two semiconductor die on the wafer;

placing the wafer, in a desired orientation, between the first plate and the second rigid plate with the plurality of contact elements on the second rigid plate engaging corresponding locations on the wafer; and

biasing the plurality of contact elements of the second rigid plate against a surface of the wafer by applying an elastic force to an opposing surface to the surface of the wafer with the first plate, the force caused by the biasing mechanism, and the force applied to substantially the entirety of the opposing surface.

2. The method as claimed in claim 1, wherein the wafer comprises a semiconductor wafer.

3. The method as claimed in claim 1, wherein the wafer includes an array of semiconductor dice located thereon.

4. The method as claimed in claim 1, further comprising:

aligning the first plate and the second rigid plate.

5. A method for performing at least one operation of a testing operation and a burn-in operation on an uncut wafer having two opposing surfaces using a first plate which

includes a biasing mechanism, and a second rigid plate selectively engageable with the first plate, the second rigid plate having a plurality of contact elements extending therefrom and having a cavity for receiving the uncut wafer therein, the method comprising:

providing a wafer having a plurality of semiconductor die thereon and a plurality of interconnects between a plurality of the semiconductor die on the wafer;

placing the wafer, in a desired orientation, between the first plate and the second rigid plate with the plurality of contact elements on the second rigid plate engaging corresponding locations on the wafer; and

biasing the plurality of contact elements of the second rigid plate against a surface of the wafer by applying an elastic force to an opposing surface to the surface of the wafer with the first plate, the force caused by the biasing mechanism, and the force applied to substantially the entirety of the opposing surface.

6. The method as claimed in claim 5, wherein the wafer comprises a semiconductor wafer.

7. The method as claimed in claim 5, wherein the wafer includes an array of semiconductor dice located thereon.

8. The method as claimed in claim 5, further comprising:

aligning the first plate and the second rigid plate.

9. A method for performing at least one operation of a testing operation and a burn-in operation on an uncut wafer having two opposing surfaces using a first plate which includes a biasing mechanism, and a second rigid plate selectively engageable with the first plate, the second rigid plate having a plurality of contact elements extending therefrom and having a cavity for receiving the uncut wafer therein, the wafer having a plurality of semiconductor die thereon and at least one interconnect between at least two semiconductor die on the wafer, the method comprising:

placing the wafer, in a desired orientation, between the first plate and the second rigid plate with the plurality of contact elements on the second rigid plate engaging corresponding locations on the wafer, at least one contact element for contacting at least a portion of the interconnect between at least two semiconductor die on the wafer; and

biasing the plurality of contact elements of the second rigid plate against a surface of the wafer by applying an elastic force to an opposing surface to the surface of the wafer with the first plate, the force caused by the biasing mechanism, and the force applied to substantially the entirety of the opposing surface.

10. The method as claimed in claim 9, wherein the wafer comprises a semiconductor wafer.

11. The method as claimed in claim 9, wherein the wafer includes an array of semiconductor dice located thereon.

12. The method as claimed in claim 9, further comprising:

aligning the first plate and the second rigid plate.

13. A method for performing at least one operation of a testing operation and a burn-in operation on an uncut wafer having two opposing surfaces using a first plate which includes a biasing mechanism, and a second rigid plate selectively engageable with the first plate, the second rigid plate having a plurality of contact elements extending therefrom and having a cavity for receiving the uncut wafer therein, the wafer having a plurality of semiconductor die thereon and having a plurality of interconnects between a plurality of semiconductor die on the wafer, the method comprising:

placing the wafer, in a desired orientation, between the first plate and the second rigid plate with the plurality of contact elements on the second rigid plate engaging corresponding locations on the wafer, a plurality of contact elements for contacting at least a portion of the plurality of interconnects between at least two semiconductor die on the wafer; and

biasing the plurality of contact elements of the second rigid plate against a surface of the wafer by applying an elastic force to an opposing surface to the surface of the wafer with the first plate, the force caused by the biasing mechanism, and the force applied to substantially the entirety of the opposing surface.

14. The method as claimed in claim 13, wherein the wafer comprises a semiconductor wafer.

15. The method as claimed in claim 13, wherein the wafer includes an array of semiconductor dice located thereon.

16. The method as claimed in claim 13, further comprising:
aligning the first plate and the second rigid plate.

17. A method for performing at least one operation of a testing operation and a burn-in operation on an uncut wafer having two opposing surfaces using a first plate which includes a biasing mechanism, and a second rigid plate selectively engageable with the first plate, the second rigid plate having a plurality of contact elements extending therefrom and having a cavity for receiving the uncut wafer therein, the wafer having a plurality of semiconductor die thereon and having a plurality of interconnects between the plurality of semiconductor die on the wafer, the method comprising:
placing the wafer, in a desired orientation, between the first plate and the second rigid plate with the plurality of contact elements on the second rigid plate engaging corresponding locations on the wafer, a plurality of contact elements for contacting at least a portion of an interconnect between at least two semiconductor die on the wafer for reducing the number of contact elements on the second rigid plate for contacting the plurality of semiconductor die on the wafer; and
biasing the plurality of contact elements of the second rigid plate against a surface of the wafer by applying an elastic force to an opposing surface to the surface of the wafer with the

first plate, the force caused by the biasing mechanism, and the force applied to substantially the entirety of the opposing surface.

18. The method as claimed in claim 17, wherein the wafer comprises a semiconductor wafer.

19. The method as claimed in claim 17, wherein the wafer includes an array of semiconductor dice located thereon.

20. The method as claimed in claim 17, further comprising:
aligning the first plate and the second rigid plate.

21. A method for performing at least one operation of a testing operation and a burn-in operation on an uncut wafer having two opposing surfaces using a first plate which includes a biasing mechanism, and a second rigid plate selectively engageable with the first plate, the second rigid plate having a plurality of contact elements extending therefrom and having a cavity for receiving the uncut wafer therein, the wafer having a plurality of semiconductor die thereon and at least one interconnect between at least two semiconductor die on the wafer, the method comprising:
placing the wafer, in a desired orientation, between the first plate and the second rigid plate with the plurality of contact elements on the second rigid plate engaging corresponding locations on the wafer, at least one contact element for contacting at least a portion of the interconnect between at least two semiconductor die on the wafer for reducing the number of contact elements on the second rigid plate for contacting the plurality of semiconductor die on the wafer; and
biasing the plurality of contact elements of the second rigid plate against a surface of the wafer by applying an elastic force to an opposing surface to the surface of the wafer with the first plate, the force caused by the biasing mechanism, and the force applied to substantially the entirety of the opposing surface.

22. The method as claimed in claim 21, wherein the wafer comprises a semiconductor wafer.

23. The method as claimed in claim 21, wherein the wafer includes an array of semiconductor dice located thereon.

24. The method as claimed in claim 21, further comprising:
aligning the first plate and the second rigid plate.